

REMARKS

Initially, Applicants wish to thank the Examiner for the detailed Office Action and for the Notice of References Cited. Further to Applicants' prior comments regarding the Information Disclosure Statement filed on September 15, 2006, Applicants note that the documents cited therein were earlier submitted for the Examiner's consideration with the Information Disclosure Statement filed on July 21, 2006 (as noted on page 2 of the Information Disclosure Statement filed on September 15, 2006) and the Examiner acknowledged consideration of each of the documents cited in the Information Disclosure Statement filed on July 21, 2006. Since the Examiner has not traversed Applicants' prior remarks (in the Office Action filed on August 7, 2009), Applicants believe that the Examiner has now concluded that the July 21, 2006 complied with the requirements for the submission of prior art, and that all of the documents have been considered.

In the outstanding Final Office Action, claims 1, 2 and 7-10 (erroneously set forth by the Examiner as claims 1, 2 and 6-10) stand rejected under 35 U.S.C. §103(a) as being unpatentable over ARIMILLI et al. (U.S. Patent No. 6,397,298) in view of "Modern Operating Systems, 2nd Edition" to Andrew S. Tanenbaum (hereinafter, "Tanenbaum"). Claims 3 and 4 stand rejected under 35 U.S.C. §103(a) as being unpatentable over ARIMILLI et al. in view of TANENBAUM, and further in view of PETTEY (U.S. Patent No. 6,021,480).

Applicants respectfully traverse the outstanding rejections. Applicants' independent claim 1 recites, *inter alia*, that the selector selects the cache entry to be replaced when a cache miss occurs and a cache entry having an oldest-order flag attached is present. Applicants' independent claim 1 further recites, *inter alia*, that the selector selects the cache entry to be replaced in accordance with the order data when the 1-bit order flag indicates that the cache entry to be replaced has been accessed since each cache entry had been reset and when the cache entry having the oldest-order flag attached is not present.

The Examiner relies on ARIMILLI et al. as teaching the claimed modifier and the claimed selector, and newly asserts TANENBAUM as disclosing the above-noted claimed combination of features. In this regard, TANENBAUM is submitted to disclose a status bit R that is set whenever a page is referenced (read or written) and a status bit M that is set when the page is written. Applicants respectfully submit that TANENBAUM also discloses that periodically, (e.g., on each clock interrupt), the R bit is cleared, to distinguish between pages that have not been referenced recently from those pages that have been recently referenced. See page 216, lines 27-29 of TANENBAUM. TANENBAUM is further submitted to disclose that the R and M bits must be updated on every memory reference; once a bit has been set to 1 it stays set to 1 until the operating system resets it to 0 in software. See page 216, lines 14-17 of TANENBAUM. The Examiner asserts that the M bit disclosed by TANENBAUM is equivalent to the claimed oldest-order flag and the R bit disclosed by TANENBAUM is equivalent to the claimed 1-bit order flag.

Applicants respectfully submit that the combination of ARIMILLI et al. in view of TANENBAUM fails to disclose or render obvious a selector that selects the cache entry to be replaced when a cache miss occurs and a cache entry having an oldest-order flag attached is present. According to a non-limiting aspect of the presently claimed invention, a weak flag W is a flag that specifies that the access order of a cache entry is regarded as the oldest. That is, W=1 means that the processor 1 reads out and writes to the cache entry no further, or that an access frequency is low. Furthermore, W=1 indicates that the access order regarding a replace control is treated as the oldest, or in other words, that it is a weakest (weak) cache entry, and W=0 indicates that such is not the case. See, e.g., page 11, lines 3-9 of Applicants' Application specification as filed (i.e., paragraph [0145] of the published application, U.S. Patent Application Publication No. 2008/0168232). TANENBAUM is submitted to merely disclose a status bit M that is set when a page is written.

Applicants respectfully submit that the combination of ARIMILLI et al. in view of TANENBAUM fails to disclose or render obvious a selector that selects the cache entry to be replaced in accordance with the order data when the 1-bit order flag indicates that the cache entry to be replaced has been accessed since each cache entry had been reset and when the cache entry having the oldest-order flag attached is not present. According to a non-limiting aspect of the presently claimed invention, a use flag U indicates whether a cache entry has been accessed, and is used at the time of a replacement due to a mishit in a least recently used (LRU) method, in place of the access order data in the cache entries of the four ways. More particularly, a use flag U of 1 indicates that an access has occurred, and 0 indicates that no access has occurred. That is, the use flag indicates two relative states, whether the time of access is old, or new. In other words, the cache entry with a use flag of 1 has been accessed more recently than a cache entry of a use flag of 0. When all use flags of the four ways in one set become 1, the use flags are reset to 0. See, e.g., page 18, line 32 to page 19, line 9 of Applicants' Application specification as filed (i.e., paragraph [0145] of the published application, U.S. Patent Application Publication No. 2008/0168232). In contrast, TANENBAUM is submitted to disclose clearing the R bit periodically, (e.g., on each clock interrupt, the R bit is cleared), to distinguish between pages that have not been referenced recently from those pages that have been recently referenced, as was noted above as being disclosed on page 216, lines 27-29 of TANENBAUM.

Even assuming, *arguendo*, that TANENBAUM were interpreted as disclosing the claimed 1-bit order flag (and Applicants submit it can not be so interpreted), the combination of ARIMILLI et al. in view of TANENBAUM as set forth by the Examiner fails to disclose a selector that selects the cache entry to be replaced in accordance with the order data when the 1-bit order flag indicates that the cache entry to be replaced has been accessed since each cache entry had been reset and when the cache entry having the oldest-order flag attached is not present.

Applicants respectfully submit that the combination of ARIMIILLI et al. in view of TANENBAUM set forth by the Examiner fails to disclose or renders obvious that the selector selects the cache entry to be replaced when a cache miss occurs and a cache entry having an oldest-order flag attached is present and that the selector selects the cache entry to be replaced in accordance with the order data when the 1-bit order flag indicates that the cache entry to be replaced has been accessed since each cache entry had been reset and when the cache entry having the oldest-order flag attached is not present, as recited in Applicants' independent claim 1.

In view of the above, Applicants respectfully submit that independent claim 1 is allowable over the combination of ARIMIILLI et al. in view of TANENBAUM for at least the reasons set forth above.

In addition, Applicants submit that the method of independent claim 10 is allowable for reasons similar to those noted above with respect to independent claim 1, in addition to reasons related to its own recitations.

Applicants respectfully submit that each of dependent claims 2 and 7-9 are allowable at least because they depend, directly or indirectly, from independent claim 1, which Applicants submit has been shown to be allowable. Each of dependent claims 2 and 7-9 are also submitted to recite further patentable subject matter. Further, arguments made above with respect to the rejection of independent claim 1 are applicable hereto for claims 3 and 4, which depend from independent claim 1. Applicants respectfully submit that each of dependent claims 3 and 4 recite further patentable subject matter and that PETTEY fails to cure the deficiencies noted above with respect to the combination of ARIMIILLI et al. in view of TANENBAUM set forth by the Examiner. As such, allowance of the dependent claims is deemed proper for at least the same reasons noted for independent claim 1 upon which they depend, in addition to reasons related to their own recitations.

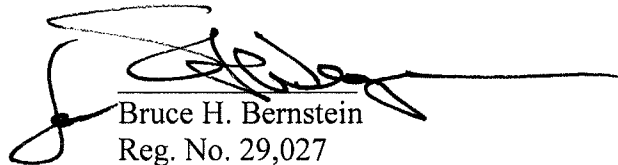
Accordingly, reconsideration and withdrawal of the rejection of claims 1, 2 and 7-10 (erroneously set forth by the Examiner as claims 1, 2 and 6-10) under 35 U.S.C. §103(a) as being unpatentable over ARIMILLI et al. in view of TANENBAUM, and the rejection of claims 3 and 4 under 35 U.S.C. §103(a) as being unpatentable over ARIMILLI et al. in view of TANENBAUM, and further in view of PETTEY is respectfully requested.

At least in view of the herein contained remarks, Applicants respectfully request reconsideration and withdrawal of each of the outstanding rejections, together with an indication of the allowability of all pending claims, in due course. Such action is respectfully requested and is believed to be appropriate and proper.

Should an extension of time be necessary to maintain the pendency of this application, the Commissioner is hereby authorized to charge any additional fee to Deposit Account No. 19-0089.

Should the Examiner have any questions, the Examiner is invited to contact the undersigned at the below-listed telephone number.

Respectfully Submitted,
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